WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

(a) a first field effect transistor, comprising:

(i) a first rail comprising a first channel region, a first gate insulating layer, and a first gate electrode,

(ii) a first source region, and

(iii) a first drain region,

(b) a second field effect transistor, comprising:

(j) a second rail comprising a second channel region, a second gate insulating layer, and a second gate electrode,

(ii) a second source region, and

(iii) a second drain region,

wherein the first rail comprises the second source region or the second drain region.

2. The device of claim 1, wherein the second rail extends in a second direction different from a first direction of the first rail.

3. The device of claim 2, further comprising a third rail extending in the first direction, wherein:

when the first rail comprises the second source region, the third rail comprises the second drain region; and

when the first rail comprises the second drain region, the third rail comprises the second source region.

4. The device of claim 3, further comprising:

a fourth rail extending in the second direction, comprising the first source region, and

a fifth rail extending in the second direction, comprising the first drain region.

5. The device of claim 4, wherein:

the first direction is substantially perpendicular to the second direction; and

the first rail and the third rail are located in a first horizontal plane between the second rail in a second horizontal plane and the fourth and fifth rails located in a third horizontal plane.

6. The device of claim 5, wherein:

the second rail is located above the first and the third rails;

the first and the third rails are located above the fourth and fifth rails;

the fourth and fifth rails are located above a substrate; and

the first and the second transistors comprise top gate staggered thin film transistors.

7. The device of claim 6, wherein the third rail comprises a gate electrode of a third field effect transistor.

8. The device of claim 5, wherein:

the first rail comprises a first heavily doped semiconductor layer of a first conductivity type and a first lightly doped semiconductor layer of a second conductivity type containing the first channel region;

the second rail comprises a second heavily doped semiconductor layer of the first conductivity type and a second lightly doped semiconductor layer containing the second channel region;

the third rail comprises a third heavily doped semiconductor layer of the first conductivity type and a third lightly doped semiconductor layer of the second conductivity type;

the fourth rail comprises a fourth heavily doped semiconductor layer of the first conductivity type; and

the fifth rail comprises a fifth heavily doped semiconductor layer of the first conductivity type.

9. The device of claim 8, wherein:

one or more of the semiconductor layers in the first through fifth rails is a polysilicon layer; and

the first and the second transistors comprise thin film transistors located above an insulating substrate or above an insulating layer formed over a silicon substrate.

10. The device of claim 9, further comprising:

a planarized insulating fill layer located between the first and the third rails and between the fourth and the fifth rails;

a first insulating isolation layer located below the first gate insulating layer in the first rail adjacent to lateral edges of the first channel region to form an island first channel region;

a second insulating isolation layer located below the second gate insulating layer in the second rail adjacent to lateral edges of the second channel region to form an island second channel region; and

a metal or a metal silicide layer located in the first through the fifth rails.

11. The device of claim 8, wherein:

the first rail further comprises a first heavily doped semiconductor layer of the second conductivity type electrically connected to the first

heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer;

the first heavily doped semiconductor layer of the second conductivity type comprises the second source region or the second drain region of the second transistor; and

the first heavily doped semiconductor layer of the first conductivity type comprises the first gate electrode of the first transistor.

12. The device of claim 11, wherein:

the second rail further comprises a second heavily doped semiconductor layer of the second conductivity type electrically connected to the second heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer;

the second heavily doped semiconductor layer of the second conductivity type comprises the second gate electrode of the second transistor;

the second heavily doped semiconductor layer of the first conductivity type comprises a drain or source region of a fourth field effect transistor; and

the second lightly doped semiconductor layer containing the second channel region is of the first conductivity type.

13. The device of claim 8, wherein:

the first gate insulating layer comprises at least a portion of a first charge storage region;

the second gate insulating layer comprises at least a portion of a second charge storage region; and

the first heavily doped semiconductor layer of the first conductivity type comprises the second source or the second drain region of the second transistor and the

first gate electrode of the first transistor.

14. The device of claim 13, wherein:

the second heavily doped semiconductor layer of the first conductivity type comprises the second gate electrode of the second transistor and a drain or source region of a fourth field effect transistor; and

the second lightly doped semiconductor layer containing the second channel region is of the second conductivity type.

15. The device of claim 14, wherein the charge storage regions comprises one of dielectric isolated floating gates, ONO dielectric films or insulating layers containing conductive nanocrystals.

16. A monolithic three dimensional array of field effect transistors, comprising:

(a) a substrate;

(b) a plurality of first rails disposed at a first height relative to the substrate in a first direction, wherein each of the plurality of first rails comprises a first heavily doped semiconductor layer of a first conductivity type;

(c) a plurality of second rails disposed in contact with the first rails, at a second height different from the first height, and in a second direction different from the first direction, wherein each of the plurality of second rails comprises a second heavily doped semiconductor layer of the first conductivity type; and

(d) a plurality of third rails disposed in contact with the second rails, in the first direction at a third height relative to the substrate such that the second rails are located between the first and the third rails,

wherein each of the plurality of third rails comprises a third heavily doped semiconductor layer of the first conductivity type;

wherein portions of the plurality of second rails comprise gate electrodes of a plurality of first field effect transistors and source or drain regions of a plurality of second field effect transistors.

17. The array of claim 16, further comprising a plurality of fourth rails disposed in the second direction at a fourth height relative to the substrate such that the third rails are located between the second and the fourth rails, wherein each of the fourth rails comprises a fourth heavily doped semiconductor layer of the first conductivity type.

18. The array of claim 17, wherein:

portions of the plurality of third rails comprise gate electrodes of the second field effect transistors and source or drain regions of a plurality of third field effect transistors;

portions of the fourth rails comprise gate electrodes of the third field effect transistors.

19. The array of claim 18, wherein:

the first and the second rails comprise a first transistor level, formed in or above the substrate, containing the plurality of first transistors;

the second and the third rails comprise a second transistor level, located above the first level, containing the plurality of second transistors; and

the third and the fourth rails comprise a third transistor level, located above the second level, containing the plurality of third transistors.

20. The array of claim 19, further comprising at least one additional transistor level monolithically formed above the third level.

21. The array of claim 16, wherein:

each of the second rails further comprises a first gate insulating layer and a first lightly doped semiconductor layer; and

each of the third rails further comprises a second gate insulating layer and a second lightly doped semiconductor layer.

22. The array of claim 21, wherein:

(a) each first field effect transistor comprises:

(i) a first gate electrode comprising a portion of one of the second rails;

(ii) a first channel region comprising a portion of the first lightly doped semiconductor layer located in the same one of the second rails;

(iii) a portion of the first gate insulating layer;

(iv) a first source region comprising a portion of one of the first rails;

(v) a first drain region comprising a portion of another one of the first rails; and

(b) each second field effect transistor comprises:

(i) a second gate electrode comprising a portion of one of the third rails;

(ii) a second channel region comprising a portion of the second lightly doped semiconductor layer located in the same one of the third rails;

(iii) a portion of the second gate insulating layer;

(iv) a second source region comprising a portion of one of the second rails; and

(v) a second drain region comprising a portion of another one of the second rails.

23. The array of claim 22, wherein:

one or more of the semiconductor layers in the first through third rails is a polysilicon layer; and

the first transistors and the second transistors comprise top gate staggered thin film transistors located above an insulating substrate or above an insulating layer formed over a silicon substrate.

24. The array of claim 22, wherein:

the first rails are formed in a single crystal silicon substrate;

the first transistors comprise bulk silicon MOSFETs;

one or more of the semiconductor layers in the second and third rails is a polysilicon layer; and

the second transistors comprise top gate staggered thin film transistors.

25. The array of claim 24, wherein a direction of the first, the second and the third rails changes over different regions of the substrate.

26. The array of claim 16, wherein:

each of the plurality of second rails further comprises:

a second lightly doped semiconductor channel layer of a second conductivity type in contact with the first rails;

a gate insulating layer between the second channel layer and the second heavily doped layer of the first conductivity type;

a second heavily doped semiconductor layer of the second conductivity type electrically connected to the

second heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer;

the second heavily doped semiconductor layer of the first conductivity type comprises a gate electrode of one of the first transistors;

the second heavily doped semiconductor layer of the second conductivity type comprises a source or drain region of one of the second transistors;

each of the plurality of third rails further comprises:

a third lightly doped semiconductor channel layer of the first conductivity type in contact with the second heavily doped layer of the second conductivity type in the second rails;

a third heavily doped semiconductor layer of the second conductivity type electrically connected to the third heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer;

a gate insulating layer between the third channel layer and the third heavily doped layer of the second conductivity type; and

the third heavily doped semiconductor layer of the second conductivity type comprises a gate electrode of one of the second transistors.

27. The array of claim 26, further comprising a plurality of vias extending through the second gate insulating layer and the second channel layer such that the third heavily doped layer of the second conductivity type contacts the second heavily doped layer of the second conductivity type through the vias.

28. The array of claim 27, wherein the vias are arranged such that at least one six transistor SRAM is formed in the array.

29. The array of claim 26, wherein gate electrodes of the first transistors of a first polarity are electrically connected to a source or drain of adjacent second transistors of a second polarity without any lateral interconnects.

30. The array of claim 26, further comprising:

a planarized insulating fill located between adjacent first rails, between adjacent second rails, and between adjacent third rails;

a first insulating isolation layer located between the first rails and the second rails;

a second insulating isolation layer located between the second rails and the third rails;

a plurality of first openings in the first isolation layers through which active regions of the second lightly doped semiconductor layers of the second conductivity type in the second rails contact the first heavily doped semiconductor layers of the first conductivity type in the first rails; and

a plurality of second openings in the second isolation layers through which active regions of the third lightly doped semiconductor layers of the first conductivity type in the third rails contact the second heavily doped semiconductor layers of the second conductivity type in the second rails.

31. The array of claim 16, wherein:

each of the second rails further comprises a second lightly doped semiconductor channel layer of a second conductivity type and a first charge storage region located between the second channel layer and the second heavily doped layer of the first conductivity type;

each of the third rails further comprises a third lightly doped semiconductor channel layer of a second conductivity type and a second charge storage region located between the third channel layer and the third heavily doped layer of the first conductivity type;

each of the second channel layers contacts the first heavily doped layer of the first conductivity type in two of the first rails; and

each of the third channel layers contacts the second heavily doped layer of the first conductivity type in two of the second rails.

32. The array of claim 31, further comprising:

planarized insulating fill located between adjacent first rails, between adjacent second rails, and between adjacent third rails; and

metal or metal silicide layers located in the first through the third rails.

wherein each second rail further comprises a first insulating isolation layer located below the first charge storage region adjacent to lateral edges of the second channel layer to form an island first channel region, and

each third rail further comprises a second insulating isolation layer located below the second charge storage region adjacent to lateral edges of the third channel layer to form an island second channel region.

33. A monolithic three dimensional array of field effect transistors, comprising:

(a) a substrate;

(b) a plurality of first rails disposed at a first height relative to the substrate in a first direction, wherein each of the plurality of first rails comprises a first heavily doped semiconductor layer of a first conductivity type;

(c) a plurality of second rails disposed at a second height different from the first height, and in a second direction different from the first direction,

wherein each of the plurality of second rails comprises:

a second lightly doped semiconductor channel layer of a second conductivity type located in contact with the first rails;

a second heavily doped semiconductor layer of the first conductivity type; and

a second gate insulating layer between and in contact with the second channel layer and the second heavily doped layer of the first conductivity type;

a second heavily doped semiconductor layer of the second conductivity type electrically connected to the second heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer;

(d) a plurality of third rails disposed in the first direction at a third height relative to the substrate, wherein each of the plurality of third rails comprises:

a third lightly doped semiconductor channel layer of the first conductivity type located in contact with the second heavily doped layer of the second conductivity type in the second rails;

a third heavily doped semiconductor layer of the second conductivity type;

a third heavily doped semiconductor layer of the first conductivity type electrically connected to the third heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer; and

a third gate insulating layer between and in contact with the channel layer and the third heavily doped layer of the second conductivity type.

34. The array of claim 33, further comprising a plurality of fourth rails disposed in the second direction at a fourth height relative to the substrate, wherein each of the plurality of fourth rails comprises:

a fourth lightly doped semiconductor channel layer of the second conductivity type in contact with the third heavily doped layer of the first conductivity type in the third rails;

a fourth heavily doped semiconductor layer of the first conductivity type; and

a fourth gate insulating layer between and in contact with the fourth channel layer and the fourth heavily doped layer of the first conductivity type; and

a fourth heavily doped semiconductor layer of the second conductivity type electrically connected to the fourth heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer.

35. The array of claim 34, wherein:

the first heavily doped semiconductor layer of the first conductivity type comprises source or a drain regions of a plurality of first transistors;

the second heavily doped semiconductor layer of the first conductivity type comprises gate electrodes of the first transistors;

the second heavily doped semiconductor layer of the second conductivity type comprises source or drain regions of a plurality of second transistors;

the third heavily doped semiconductor layer of the second conductivity type comprises gate electrodes of the second transistors; and

the third heavily doped semiconductor layer of the first conductivity type comprises source or drain regions of a plurality of third transistors.

36. The array of claim 35, wherein:

one or more of the semiconductor layers in the first through fourth rails is a polysilicon layer; and

the pluralities of first, second and third transistors comprise top gate staggered thin film transistors located above an insulating substrate or above an insulating layer formed over a silicon substrate.

37. The array of claim 36, further comprising:

planarized insulating fill located between adjacent first rails, between adjacent second rails, between adjacent third rails, and between adjacent fourth rails;

a first insulating isolation layer located between the first rails and the second rails;

a second insulating isolation layer located between the second rails and the third rails;

a third insulating isolation layer located between the third rails and the fourth rails;

a plurality of first openings in the first isolation layers through which the second lightly doped semiconductor layers of the second conductivity type in the second rails contact the first heavily doped semiconductor layers of the first conductivity type in the first rails;

a plurality of second openings in the second isolation region through which the third lightly doped semiconductor layers of the first conductivity type in the third rails contact the second heavily doped

semiconductor layers of the second conductivity type in the second rails; and

a plurality of third openings in the third isolation layer through which the fourth lightly doped semiconductor layers of the second conductivity type in the fourth rails contact the first heavily doped semiconductor layers of the first conductivity type in the first rails.

38. A semiconductor device, comprising:

a first field effect transistor of a first polarity; and

a second field effect transistor of a second polarity;

wherein a gate electrode of the first transistor is electrically connected to a source or drain of the second transistor without any lateral interconnects.

39. A monolithic three dimensional memory array of field effect transistors, comprising:

(a) a substrate;

(b) a plurality of first rails disposed at a first height relative to the substrate in a first direction, wherein each of the plurality of first rails comprises a first heavily doped semiconductor layer of a first conductivity type;

(c) a plurality of second rails disposed in contact with the first rails at a second height different from the first height, and in a second direction different from the first direction, wherein each of the plurality of second rails comprises:

a second heavily doped semiconductor layer of the first conductivity type;

a second lightly doped semiconductor channel layer of the second conductivity type; and

a second charge storage region located between the second heavily doped semiconductor layer and the second lightly doped semiconductor layer; and

(d) a plurality of third rails disposed in the first direction at a third height relative to the substrate such that the second rails are located between the first and the third rails, wherein each of the plurality of third rails comprises:

a third heavily doped semiconductor layer of the first conductivity type;

a third lightly doped semiconductor channel layer of the second conductivity type; and

a third charge storage region located between the third heavily doped semiconductor layer and the third lightly doped semiconductor layer;

wherein:

the second lightly doped semiconductor layers in the second rails contact the first heavily doped semiconductor layers in the first rails; and

the third lightly doped semiconductor layers in the third rails contact the second heavily doped semiconductor layers in the second rails;

40. The array of claim 39, further comprising:

a first insulating isolation layer located between the first rails and the second rails;

a plurality of first openings located in the first insulating isolation layer;

a second insulating isolation layer located between the second rails and the third rails; and

a plurality of second openings located in the second insulating isolation layer.

41. The array of claim 40, wherein:

a plurality of first transistor channel islands comprise portions of the second lightly doped semiconductor layers located in the first openings;

the first transistor channel islands contact the first heavily doped semiconductor layers in the first rails;

first transistor bit lines comprise the first heavily doped semiconductor layers in the first rails;

first transistor word lines comprise the second heavily doped semiconductor layers in the second rails;

a plurality of second transistor channel islands comprise portions of the third lightly doped semiconductor layers located in the second openings;

the second transistor channel islands contact the second heavily doped semiconductor layers in the second rails;

second transistor bit lines comprise the second heavily doped semiconductor layers in the second rails; and

second transistor word lines comprise third heavily doped semiconductor layers in the third rails.

42. The array of claim 41, further comprising:

a plurality of fourth rails disposed in contact with the third rails at a fourth height in the second direction, wherein each of the plurality of fourth rails comprises:

a fourth heavily doped semiconductor layer of the first conductivity type;

a fourth lightly doped semiconductor layer of the second conductivity type; and

a fourth charge storage region located between the fourth heavily doped semiconductor layer and the fourth lightly doped semiconductor layer.

43. The array of claim 42, wherein:

the first rails are monolithically located above the substrate;

the second rails are monolithically located on the first rails;

the third rails are monolithically located on the second rails;

the fourth rails are monolithically located on the third rails;

the first and the second rails comprise a first transistor level, formed in or above the substrate, containing a plurality of first transistors; and

the second and the third rails comprise a second transistor level, located above the first level, containing a plurality of second transistors.

44. The array of claim 43, wherein:

a predetermined transistor of the memory array is programmed by applying a high programming voltage to the transistor's word line, grounding the transistor's bit lines and applying a low programming inhibiting voltage to unselected word lines and bit lines;

a predetermined transistor of the memory array is erased by applying a high erase voltage to the transistor's bit lines, grounding the transistor's word line and applying a low erase inhibiting voltage to the word lines in the same transistor level as the predetermined transistor's word line and to the bit lines in the same transistor level as the predetermined transistor's bit lines; and

a predetermined transistor of the memory array is read by applying a first low read voltage to the transistor's word line, applying a second read voltage which is lower than the first read voltage to the transistor's bit lines, allowing the word lines in the same transistor level as the predetermined transistor's word line and the bit lines in the same transistor level as the predetermined transistor's bit lines to float, and sensing a current between the predetermined transistor's bit lines.

45. The array of claim 44, wherein a predetermined block of transistors in a predetermined level of the memory array is erased by applying a high erase voltage to all bit lines in the block, grounding word lines in the block and applying a low erase inhibiting voltage to or grounding word lines and bit lines outside of the predetermined block.

46. A method of programming a selected transistor in the array of claim 43, comprising:

applying a high programming voltage to the selected transistor's word line;

grounding the selected transistor's bit lines; and

applying a low programming inhibiting voltage to unselected word lines and bit lines.

47. A method of erasing a selected transistor of the array of claim 43, comprising:

applying a high erase voltage to the selected transistor's bit lines;

grounding the selected transistor's word line; and

applying a low erase inhibiting voltage to other word lines in the same transistor level as the selected transistor's word line and to the other bit lines in the same transistor level as the selected transistor's bit lines.

48. A method of reading a selected transistor of the array of claim 43, comprising:

applying a first low read voltage to the selected transistor's word line;

applying a second read voltage which is lower than the first read voltage to the selected transistor's bit lines;

allowing the word lines in the same transistor level as the selected transistor's word line and the bit lines in the same transistor level as the selected transistor's bit lines to float; and

sensing a current between the selected transistor's bit lines.

49. A method of erasing a block of transistors of the array of claim 43, comprising:

applying a high erase voltage to all bit lines in the block;

grounding word lines in the block; and

applying a low erase voltage to or grounding word lines and bit lines outside of the block to be erased.

50. A method of making a monolithic three dimensional field effect transistor array, comprising:

forming a plurality of first rails disposed at a first height relative to a substrate in a first direction, wherein each of the plurality of first rails comprises a first heavily doped semiconductor layer of a first conductivity type;

forming a first insulating isolation layer over the first plurality of rails;

patterning the first isolation layer to form a plurality of first openings exposing upper portions of adjacent first rails;

forming a second lightly doped semiconductor layer of a second conductivity type over the patterned isolation layer such that transistor channel portions in the second lightly doped layer of the second conductivity type contact the first heavily doped layer of the first conductivity type through the first openings;

forming a second gate insulating layer over the second lightly doped semiconductor layer of the second conductivity type;

forming a second heavily doped semiconductor layer of the first conductivity type over the second gate insulating layer; and

patterning the second heavily doped layer of the first conductivity type, the second gate insulating layer, and the second lightly doped layer of the second conductivity type to form a plurality of second rails extending in a second direction different from the first direction.

51. The method of claim 50, further comprising:

forming a second insulating isolation layer over the plurality of second rails;

patterning the second isolation layer to form a plurality of second openings exposing upper portions of adjacent second rails;

forming a third lightly doped semiconductor layer over the patterned second isolation layer such that transistor channel portions of the second lightly doped layer contact the second rails through the second openings;

forming a third gate insulating layer over the third lightly doped semiconductor layer;

forming a third heavily doped semiconductor layer over the third gate insulating layer; and

patterning the third heavily doped layer, the third gate insulating layer and the third lightly doped layer to form a plurality of third rails extending in the first direction.

52. The method of claim 51, further comprising forming a plurality of fourth rails extending in the second direction in contact with the third rails.

53. The method of claim 51, further comprising:

forming a first insulating fill layer between adjacent first rails;

polishing the first insulating fill layer to expose the first rails using the first rails as a polish stop;

forming a second insulating fill layer between adjacent second rails;

polishing the first insulating fill layer to expose the second rails using the second rails as a polish stop;

forming a third insulating fill layer between adjacent third rails; and

polishing the third insulating fill layer to expose the third rails using the third rails as a polish stop.

54. The method of claim 53, wherein the step of forming the first rails further comprises:

forming a second heavily doped polysilicon layer over the substrate;

forming a first metal or metal silicide layer over the second polysilicon layer;

forming the first heavily doped semiconductor layer on the first metal or metal silicide layer; and

patterning the first semiconductor layer and the second polysilicon layer and the first metal or metal silicide layers.

55. The method of claim 51, wherein:

the third lightly doped semiconductor layer comprises a third lightly doped amorphous silicon or polysilicon layer of the first conductivity type; and

the third heavily doped semiconductor layer comprises a third heavily doped polysilicon layer of the second conductivity type formed on the third gate insulating layer.

56. The method of claim 55, further comprising:

forming a second metal or metal silicide layer on the second heavily doped semiconductor layer of the first conductivity type;

forming a second heavily doped semiconductor layer of the second conductivity type on the second metal or metal silicide layer;

patterning the second metal or metal silicide layer and the second heavily doped semiconductor layer of the second conductivity type during the step of patterning to form the second rails;

forming a third metal or metal silicide layer on the third heavily doped polysilicon layer of the second conductivity type;

forming a third heavily doped semiconductor layer of the first conductivity type on the third metal or metal silicide layer; and

patterning the third metal or metal silicide layer and the third heavily doped semiconductor layer of the first conductivity type during the step of patterning to form the third rails.

57. The method of claim 56, wherein all layers in the second rails are patterned by etching during one etching step.

58. The method of claim 56, further comprising:

forming vias which extend through the second gate insulating layer and the second lightly doped layer to the first rails;

depositing the second heavily doped layer of the first conductivity type into the vias such that the second heavily doped layer of the first conductivity type contacts the first heavily doped layer of the first conductivity type;

forming vias which extend through the third gate insulating layer and the third lightly doped layer to the second rails; and

depositing the third heavily doped layer of the second conductivity type into the vias such that the third heavily doped layer of the second conductivity type contacts the second heavily doped layer of the second conductivity type.

59. The method of claim 51, wherein:

the third lightly doped semiconductor layer comprises a third lightly doped amorphous silicon or polysilicon layer of the second conductivity type;

the third heavily doped semiconductor layer comprises a third heavily doped polysilicon layer of the first conductivity type formed on the third gate insulating layer.

60. The method of claim 59, further comprising:

forming a second metal or metal silicide layer on the second heavily doped semiconductor layer of the first conductivity type;

forming a fourth heavily doped semiconductor layer of the first conductivity type on the second metal or metal silicide layer;

patterning the second metal or metal silicide layer and the fourth heavily doped semiconductor layer of the first conductivity type during the step of patterning the second rails;

forming a third metal or metal silicide layer on the third heavily doped polysilicon layer of the first conductivity type;

forming a fifth heavily doped semiconductor layer of the first conductivity type on the third metal or metal silicide layer; and

patterning the third metal or metal silicide layer and the fifth heavily doped semiconductor layer of the first conductivity type during the step of patterning the third rails.

61. The method of claim 50, wherein all layers in the second rails are patterned by etching during one etching step.

62. A monolithic three-dimensional array of active devices comprising odd and even levels of field effect transistors, wherein:

odd levels comprise transistors of a first polarity;

even levels comprise transistors of a second polarity;

each transistor comprises a gate electrode, source, and drain, wherein the gate electrodes, sources, and drains of the transistors of at least two levels comprise polysilicon;

current flows between the source and the drain in a first direction through transistors of the first polarity; and

current flows between the source and the drain in a second direction not parallel to the first direction through transistors of the second polarity.

63. The array of claim 62, further comprising:

a substrate;

a plurality of first rails disposed at a first height above the substrate, extending in the first direction, said plurality of first rails comprising sources and drains of the first level of the transistors;

a plurality of second rails in contact with the first rails, at a second height different from the first height, extending in a second direction, said second rails comprising gate electrodes of the first level of transistors and further comprising sources and drains of the second level of transistors; and

a plurality of third rails in contact with the second rails, at a third height different from the second height, extending in the first direction, such that the second rails are located between the first rails and the third rails, said third rails comprising gate electrodes of the second level of transistors.

64. The array of claim 63, wherein the second direction is substantially orthogonal to the first direction.

65. A semiconductor device, comprising:

a first transistor having a gate electrode, source, channel, and drain oriented in a first direction;

a second transistor having a gate electrode, source, channel, and drain oriented in a second direction different from said first direction; and

wherein the gate electrode of said first transistor and the source of said second transistor are disposed in a portion of a first rail.

66. The device of claim 65, wherein the first direction is substantially orthogonal to the second direction.

67. The device of claim 66, wherein the channel of the first transistor is located at a first height and the channel of the second transistor is located at a second height different from the first height.

68. The device of claim 67, wherein:

the first rail comprises the channel of the first transistor and extends in the first direction; and

a second rail comprises a source or drain of the first transistor and extends in the second direction.

69. A semiconductor device comprising a first rail, said first rail comprising:

a gate electrode of a first field effect transistor; and

a source or drain of a second field effect transistor;

wherein said first transistor and said second transistor are oriented in non-parallel directions.

70. The device of claim 69, wherein:

the first transistor further comprises:

a first source; and

a first drain; and

the second transistor further comprises:

a second gate electrode; and

a second drain or source.

71. The device of claim 70, wherein:

the second gate electrode comprises a portion of a second rail extending in a second direction different from a first direction of the first rail;

the second drain or source comprises a portion of a third rail extending in the first direction;

the first source comprises a portion of a fourth rail extending in the second direction, and

the first drain comprises a portion of a fifth rail extending in the second direction.

72. The device of claim 71, wherein:

the first direction is substantially perpendicular to the second direction; and

the first rail and the third rail are located in a first horizontal plane between the second rail in a second horizontal plane and the fourth and fifth rails located in a third horizontal plane.